Methods for Sensing Wearouts of Electronic Circuits

Approaches to analyze circuit-level reliability and evaluate the lifetime of complex systems

Georgia Tech inventors have developed several approaches to analyze circuit-level reliability and evaluate the lifetime of complex systems. Their methodologies involve diagnosing wear out in static random access memory (SRAM) array and to monitor the system health using diagnosis results.The novelty of the work, with regards to microprocessors, is statistical timing analyzer and the ability to handle a variety of front end of line wear out mechanisms. This includes the manufacturing process variability and the real-time uncertainties in workload and ambient conditions, like operating temperature and IR drops. The technology presents a correlation between circuit performance (speed) and circuit lifetime, which enables circuit designers to avoid excessive guard-banding by using a better, reliable, budget to achieve higher performance.With regards to SRAMs, parts of the technology implement built-in self-test system and statistical analysis methodologies for electrical detection and diagnosis of wear out mechanisms. The method uses the embedded SRAM as a monitor of system health. The bit failures are tracked with error correcting code and the cause of failure is diagnosed with on-chip built-in self-test system. The wear out model parameters are estimated from the diagnosis results and combined with system wear out simulator to estimate the remaining lifetime of the entire processor. This work has been proposed with a variety of approaches, including electrical system design, statistical analysis, and developing new simulation workflows.

Summary Bullets

- Circuit details are taken into account in estimating lifetime
- Wearout methods can be used to determine “timing closure” at 10 years lifetime
- Methods serve as foundation for a new electronic design automation tool for “timing closure”

Solution Advantages

- Circuit details are taken into account in estimating lifetime
- Wearout methods can be used to determine “timing closure” at 10 years lifetime
- Methods serve as foundation for a new electronic design automation tool for “timing closure”
- Proactive system; aims to detect failures in advance through remaining life estimates
- System does not rely on multiple copies of circuitry, saving power and cost
- Electrical diagnosis identifies the failing cell, site within the cell, and the faulty mechanism

Potential Commercial Applications

- Electronic design automation tool for electrical fault diagnosis
- Toolset to determine “timing closure” of semiconductor integrated circuits design and systems

Background and More Information

The scaling of semiconductor integrated circuit process technologies involves the reduction of interconnect and transistor dimensions without reducing the supply voltage. Unfortunately, the wear out of transistor devices and interconnects is occurring more quickly. Attempts to estimate the remaining lifetime and reliability of integrated circuits have focused on operating parameters, such as temperature, voltage, and operating frequency. The operating parameters are monitored using embedded sensors, which require additional components and circuitry. These sensors do not have the capability to diagnose failure mechanisms within the integrated circuit.There is a technology need to reduce power consumption, size, and cost of electronic circuits as well as to detect failures within them.

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