Heterogeneous Interconnect Geometries in Electronic Packages

A variable interconnect geometry with increased electrical performance

Georgia Tech researchers have developed a variable interconnect geometry formed on a substrate that allows for increased electrical performance of the interconnects without compromising mechanical reliability. The compliance of the interconnects varies from the center of the substrate to edges of the substrate. The variation in compliance can either be step-wise or continuous. Exemplary low-compliance interconnects include columnar interconnects and exemplary high-compliance interconnects include helix interconnects. A cost-effective implementation using batch fabrication of the interconnects at a wafer level through sequential lithography and electroplating processes may be employed.

Summary Bullets

- Increased electrical performance of the interconnects
- Does not compromise mechanical reliability
- Cost effective

Solution Advantages

- Increased electrical performance of the interconnects
- Does not compromise mechanical reliability
- Cost effective
- Effective power distribution design and thermal management solutions

Potential Commercial Applications

- High performance microprocessors and computers

Background and More Information

Conventional electronic packages typically include interconnects that are nearly identical in shape and size from the center to the edge. Flip chip solder bumps, BGA solder balls and CSP interconnects are some of the examples. However, as one moves from the center to the edge of a package or a chip, the conditions change - the interconnect at the furthest distance from the center of the die, where the differential displacement between the

die and the substrate due to CTE mismatch is maximum, has sufficient fatigue life and will not delaminate or crack the low-K dielectric in the die.

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