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Efficient, Reliable, Robust Power Amplifiers for **Wireless Communications**

A dynamically adaptive class-E switching power amplifier with duty cycle modulation

Researchers at Georgia Tech have developed a dynamically adaptive class-E switching power amplifier with duty cycle modulation. Designed in an advanced 65-nm complementary metal oxide semiconductor (CMOS) process for 2.4-GHz carrier frequency, this new technology uses an inductor-capacitor (LC) tuning circuit with a variable capacitor. This simple tuning network uses only one tunable capacitor with a certain tuning range, while the capacitor is tuned in a static way or dynamically at the rate of the envelope signal only.

Compared to existing products, Georgia Tech's innovation improves efficiency at lower power levels, enhances reliability through reductions in peak drain voltage, and mitigates process variation effects. The tuning network is much simpler than that in other adaptive power amplifiers.

Summary Bullets

- **Increased efficiency** Satisfies zero voltage switching condition at 50% duty cycle and shapes the drain voltage at other duty cycles to minimize power loss
- Improved reliability Reduces peak drain swing
- Mitigated variation Determines optimal adaptation settings for each process shifted device using onchip sensors and digital logic

Solution Advantages

- **Increased efficiency** Satisfies zero voltage switching condition at 50% duty cycle and shapes the drain voltage at other duty cycles to minimize power loss
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Potential Commercial Applications

- Mobile handsets and other portable devices
- Base station applications
- Wireless communication products

Background and More Information

This technology was developed to ensure high efficiency levels and to address process variation and reliability effects for power amplifiers used in radio frequency (RF) communication systems. Integrated power amplifiers for RF systems operate at large power back-off while enduring intense process variation and high signal levels, all of which reduces efficiency, degrades performance, and negatively impacts reliability. Efforts to address these challenges traditionally have included modifying power amplifier circuits and various efficiency improvement techniques. The current trend is to design an adaptive power amplifier and tune it using on-chip digital logic or a digital signal processor to ensure high efficiency at all output power levels. Unfortunately, these designs are complex and/or use multiple tunable capacitors. Georgia Tech has developed a better tuning network for adaptive power amplifiers.

Inventors

- Dr. Aritra Banerjee Analog Design Engineer - Kilby Labs, Texas Instruments
- Dr. Abhijit Chatterjee Professor - Georgia Tech School of Electrical and Computer Engineering

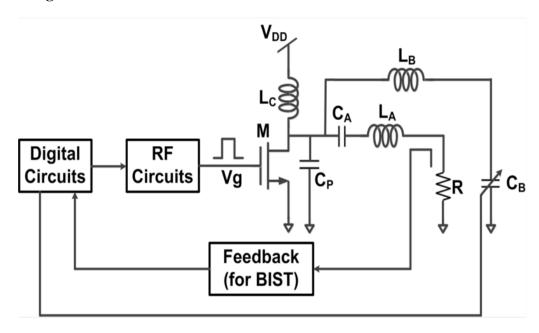
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