Fine-Pitch Chip-to-Substrate Interconnect Assemblies for Advanced Electronics Applications (#4878)

Bonding mechanism to join copper bumps on flip-chips to substrates

This new technique for interconnected assemblies overcomes the limitations of solder bumps in electronic systems, enabling shorter interconnections, fine pitch, and higher input/output (I/O) density. An adhesive bonding mechanism replaces solder technology in chip-package interconnects to join flip-chip copper bumps to organic or inorganic substrate materials.

The copper bumps connect with the pads on the substrate so as to power the circuits on the die. Before assembly, the adhesive material is heated into a gel-like structure, which allows the copper bumps to pierce through it and connect with the substrate pads. Following assembly, the adhesive is reheated and cured to form a stable, rigid polymer that holds the assembly together.

Adhesive bonding is widely used with gold bumps and inorganic substrates, but Georgia Tech's method is the first to demonstrate the reliability of using industry-standard copper bumps on both inorganic and organic substrates.

Benefits/Advantages

- **Secure**: Forms a mechanical locking structure via the bump and substrate deformation
- **Strong**: Relies on compressive stresses developed during the adhesive curing process to create the connection between chip bumps and substrate pads
- **Economical**: Costs significantly less than interconnect assemblies made with gold bumps
- **Reliable**: Enables processing flip-chip interconnects at fine pitch in next-generation electronic systems

Potential Commercial Applications

Flip-chip bumping technology is especially suitable for high-speed, high-frequency, I/O applications such as:

- Semiconductor interconnection assemblies
- Chip-to-substrate interconnect assemblies
- 3D electronic systems

Background/Context for This Invention

In the continuous drive to achieve small form-factor packages, chip-to-substrate interconnect devices have evolved from conventional solder-based techniques. As microelectronic systems trend toward higher functionality with ever-decreasing dimensions, the miniaturization of electrical systems requires passive components and active devices to be integrated on a single platform at both micro- and nano-scales.

One interconnect solution involves chip-to-substrate interconnect assemblies that utilize flip-chip technology. In general, solder bumps are placed on an active surface of a chip, and the chip is subsequently flipped so that the solder bumps can be connected to a substrate pad. The geometry of the interconnection, however, can reduce the bump pitch or density and limit reliability. Electro-migration issues and intermetallic formations pose additional concerns. For these reasons, there is a need for a fine-pitch chip-to-substrate interconnect assembly that is compatible with flip-chip technology, less costly than gold interconnects, and can handle increased I/O density.

Georgia Tech’s innovation uses an adhesive bonding mechanism for joining the chip to its packaging with copper bumps, thereby increasing the stability and reliability of the assembly while reducing costs.

Nitesh Kumbhat
Former Research Program Manager - Georgia Institute of Technology

Abhishek Choudhury
Former Grad Student - Georgia Institute of Technology

Dr. Venky Sundaram
Professor - Georgia Tech School of Electrical and Computer Engineering

Dr. Rao R. Tummala
Distinguished and an Endowed Chair Professor - Georgia Tech Computer Engineering and Materials Science and Engineering

More Information

U.S. Patent Issued - 8,633,601

Publications

A cross-section of an interconnect assembly

For more information about this technology, please visit:
https://licensing.research.gatech.edu/technology/fine-pitch-chip-substrate-interconnect-assemblies-advanced-electronics-applications