Chemical Etching of Semiconductive Substrate

Simple method using etching of substrates to produce nanostructures

Researchers at Georgia Tech have developed a technique to produce uniform micro-nanostructures on silicon simply by employing a sputtering technique to deposit catalysts. The morphology of the catalysts can be easily controlled by the sputtering rate and duration. Careful control of the catalysts' morphology can produce uniform high-aspect ratio structures with lateral size below 1 micro m could be fabricated with high speed. The technology is virtually able to produce TSVs on much larger substrate within similar duration due to its nature of wet etching.

Summary Bullets

- **Quick –** wafers can be processed in parallel, as compared to only one at a time with the current approach
- **Low cost –** tooling for this approach is much less expensive than that required for the currently used method; simple, inexpensive chemical

Solution Advantages

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Potential Commercial Applications

- Semiconductor advance packaging
- Fabricating microelectromechanical systems (MEMS)

Background and More Information

Metal-assisted chemical etching (MaCE) has been proposed as a promising silicon etching technology that is applicable in fabrication of through silicon vias (TSVs), micro electromechanical systems (MEMS) and many other components in modern microelectronic systems with high aspect ratio, high uniformity, and low cost. Typical MaCE process involves standard lithography, followed by metal deposition and subsequent etching in wet solution. The morphology of metal catalyst is critical to the final etching profile. Previously, electron-beam evaporation has been used to deposit gold catalyst in order to obtain uniform MaCE. However, long pumping time is required for EBE in each batch of production, thus slowing down the speed of overall production by

MaCE. Furthermore, the influence of catalysts morphology has not been fully investigated.

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Publications

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