Georgia | Research Tech | Corporation

Technologies

Available for LICENSING

OFFICE OF TECHNOLOGY LICENSING

https://licensing.research.gatech.edu | techlicensing@gtrc.gatech.edu

Self-Aligned HARPSS Micromechanical Variable Capacitors

A silicon micro-fabrication technique for the implementation of tunable capacitors with very small tuning voltages

Inventors at Georgia Tech have developed a modified HARPSS fabrication process to implement one-port and two-port tunable capacitors, micromachined accelerometers, gyroscopes, resonators and filters. This self-aligned HARPSS fabrication process offers the possibility of having the sub-micron capacitive HARPSS gap together with several self-aligned gaps, which were not available using other bulk micromachining processes. Disclosed are one-port and two-port microelectromechanical structures including variable capacitors, switches, and filter devices. High aspect-ratio micromachining is used to implement low-voltage, large value tunable and fixed capacitors, and the like. Tunable capacitors can move in the plane of the substrate by the application of DC voltages and achieve greater than 240 percent of tuning.

Summary Bullets

- Results in larger-value capacitors
- Requires only three lithography masks

Solution Advantages

- Results in larger-value capacitors
- Requires only three lithography masks

Potential Commercial Applications

- Tunable capacitors
- Bulk micromachined resonators and filters
- Accelerometers and gyroscopes

Background and More Information

Large-value tunable and/or variable capacitors are needed in a variety of applications, including low-frequency tunable filters and electrostatic energy harvesting devices. Although there exist several high-performance capacitors using different fabrication technologies, low actuation voltage tunable capacitors with large values are

not available in small form-factor. High aspect ratio poly silicon and single crystal silicon (HARPSS) fabrication technique was previously developed for implementation of high-Q low-voltage one-port capacitors on SOI substrate, but it does not offer two different gap sizes required for tunable capacitors without any lithographic misalignment error.

Inventors

- Dr. Farrokh Ayazi Professor and Director of Integrated MEMS (IMEMS) Laboratory – Georgia Tech School of Electrical and Computer Engineering
- Dr. Mina Rais-Zadeh Graduate Research Assistant – Georgia Tech School of Electrical and Computer Engineering (Now at NASA Jet Propulsion Laboratory)
- Pezhman Monadgomi Senior Design and Process Engineer - Silicon Clocks

IP Status

: US7977136

Publications

, -

Images



Visit the Technology here: Self-Aligned HARPSS Micromechanical Variable Capacitors https://s3.sandbox.research.gatech.edu//index.php/print/pdf/node/3583